32.6 A 1.8V 165mW Discrete Wavelet Multi-Tone Baseband Receiver for Cognitive Radio Applications

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As wireless applications become more and more sophisticated and pervasive, it is expected that the demand for bandwidth will increase substantially. Recently, several studies indicated that "on the average" the utilization of allocated spectrum is actually quite low. Thus, it is desirable to have a "cognitive" communication system that has the ability to efficiently exploit unused spectrum. Such technology is called cognitive radio (CR) [1]. In light of this, IEEE recently formed the 802.22 standards committee to work on a CR standard for wireless regional area networks [2].

Spectrum sensing and modulation that supports flexible spectrum assignment and low adjacent channel leakage are indispensable for CR systems. OFDM that can disable the sub-bands occupied by legitimate users is quite suitable for CR systems. A CR system operating in the 5GHz band and using OFDM modulation is reported in [3]. However, in several popular bands where the unoccupied spectrum is divided into many fragments of various sizes, e.g. GSM and TV bands, high leakage caused by the sidelobes makes OFDM undesirable for CR applications. On the other hand, discrete wavelet multitone (DWMT) modulation [4] uses signaling waveforms longer than that in OFDM and thus has much lower adjacent channel leakage (see Fig. 32.6.1).

A DWMT-based CR system is presented that operates in the GSM band, and an associated baseband receiver using a wavelet compatible with the exponentially-modulated filter bank (EMFB) [5] is designed and implemented. Fig. 32.6.2 shows the block diagram of the proposed DWMT-based CR system. It consists of a GSM transceiver, a main control block, and a CR transceiver (analog front-end and digital baseband). The GSM transceiver listens to the broadcast control channel (BCCH) in the GSM system and obtains a GSM channel configuration. In addition, this transceiver establishes a control channel between the CR access point (AP) and the CR mobile terminals (MT). The main control block handles detection of available GSM sub-bands and the operation of the CR control channel. The proposed CR system targets the GSM uplink band (890 to 915MHz) and the GSM downlink band (935 to 960MHz). The digital baseband operates at a 25.6MHz sampling rate and the DWMT modulation provides 256 sub-bands with 100kHz spacing. The sub-band signal main-lobe is 200kHz wide, which fits the GSM sub-bands perfectly. Binary, quaternary, and 8-level PAM signals can be transmitted on each sub-band, making the achievable uncoded bit rate at 51.2, 102.4 and 153.6Mb/s, respectively.

In the digital baseband transmitter, an exponentially-modulated synthesis bank (EMSB), the synthesis part of EMFB, implements the DWMT modulation. In the baseband receiver, a carrier frequency offset (CFO) estimator derives the coarse CFO from received preamble samples. Because the preamble in a packet is periodic with a period of 128 samples, delay correlation of 128-sample delay is computed and the phases of the correlation results are averaged to estimate the coarse CFO. The CFO is then compensated by a CFO de-rotator and the sampling clock offset (SCO), assumed proportional to CFO, is also compensated. The symbol timing estimator determines symbol timing by matching the received samples against the known preamble waveform. An exponentially-modulated analysis bank (EMAB) then realizes the DWMT demodulation. The arrangement of the training symbols avoids inter-sub-band and inter-symbol interferences in the received DWMT signal to facilitate robust channel estimation. The estimated channel responses are applied in a frequency-domain equalizer (FEQ) to restore signals that have been corrupted by multi-path fading in wireless channels. Finally, the received pilot sub-band signals in the data symbols are extracted to estimate the frequency error, which can then be combined with the coarse CFO and used in CFO/SCO compensation.

Figure 32.6.3 shows the circuit diagrams of CFO estimator, symbol timing estimator, FEQ, and frequency error detector. Delay lines in the CFO estimator, shared with EMAB, are for delay correlation and moving average. The phase of the delay correlator peak is then computed, and the results are accumulated and normalized to estimate the coarse CFO. The symbol timing estimator uses a 128-tap matched filter, whose output maximum indicates the symbol timing. Each tap has four XOR gates for 1b complex multiplication. Two specialized Wallace trees then sum partial products. In the FEQ, equalizer coefficients are computed using a pipelined divider that divides the complex conjugate of a channel gain by the power of that gain. In the frequency error detector, a shared divider computes the normalized pilot power, which is used as the weight for that pilot. Another shared arctangent circuit derives the pilot phase, whose difference between two symbols is computed. A multiplier-and-accumulator then computes the frequency error using a weighted average. The above circuit design techniques save 21% logic and 60% memory complexity.

The EMAB is the key module of the baseband receiver and in [5] an efficient decomposition, containing two lattice operations, one discrete cosine transform (DCT) and one discrete sine transform (DST), is presented. In this design, the lattice section, FFT butterfly units, and twiddle-factor complex multipliers are shared in the EMAB block (see Fig. 32.6.4). A novel bi-directional first-in-first-out (FIFO)/last-in-first-out (LIFO) circuit is designed and it can be used either as a stack and a FIFO or two stacks. Moreover, sub-band constant multiplications contained in the post-FFT processing can be eliminated without incurring any degradation. This is because the constants will be absorbed in the estimated channel responses. Further common term extraction also saves several adders, multipliers, and ROMs. Finally, the bit reversal operation in the FFT is unnecessary since the active sub-bands in a CR system are already quite dynamic and thus processing the sub-band data in sequence is unnecessary. The hardware reduction techniques used in the EMAB design are illustrated in Fig. 32.6.5. In summary, 52% of logic and 26% of memory complexity are saved through the above circuit techniques.

Figure 32.6.6 shows the schmoo plot, measured bit error rate (BER) results and chip summary. The baseband receiver integrated 267K logic gates and 60Kb SRAM in a 2.5×2.5mm^2 core size using 0.18μm CMOS technology. Test results show that the core draws 165mW from a 1.8V power supply while running at 25.6MHz. The BER performance of the proposed receiver with under 20ppm synchronization errors and a perfectly-synchronized OFDM receiver, both operating in multi-path Rayleigh fading channels, are plotted. With only 1 to 2dB degradation, the DWMT receiver performance is comparable to that of the ideal OFDM receiver. The chip micrograph is shown in Fig. 32.6.7.

Acknowledgments:
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References:
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[2] http://www.ieee802.org/22/, IEEE 802.22 WRAN WG Website.
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[4] M. A. Trannes, et al., "DMT Systems, DWMT Systems and Digital Filter Banks," *Proc. ICC*, vol. 1, pp. 311-315, May, 1994.
[5] J. Alhava, A. Viholainen, and M. Renfors, "Efficient Implementation of Complex Exponentially-Modulated Filter Banks," *IEEE Proc. ISCAS*, pp. IV-157-IV-160, May, 2003.

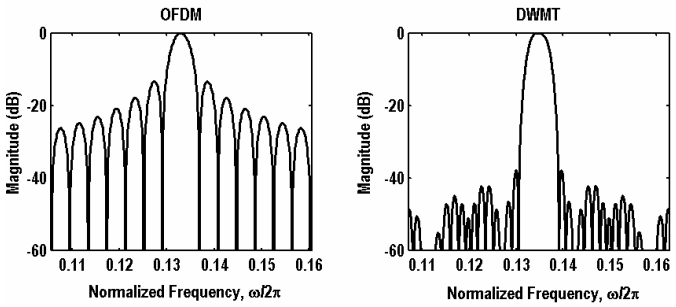


Figure 32.6.1: Spectra of typical OFDM and DWMT signals.

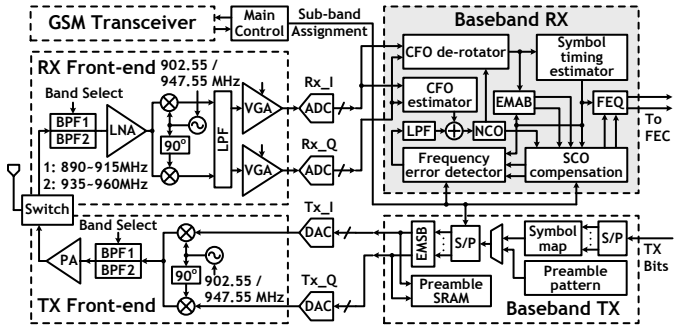


Figure 32.6.2: Block diagram of the DWMT-based CR system.

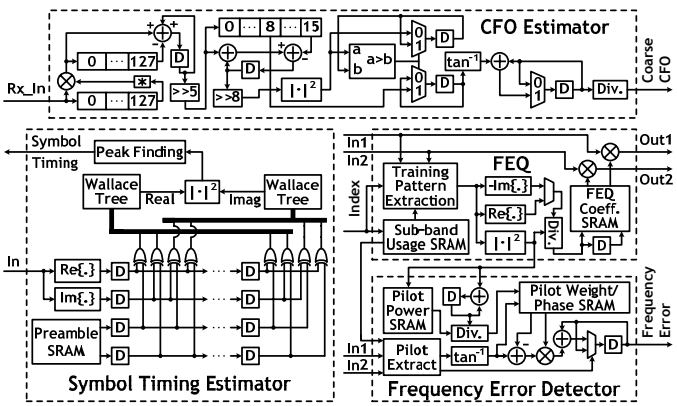


Figure 32.6.3: Circuit diagrams of CFO estimator, symbol timing estimator, FEQ, and frequency error detector.

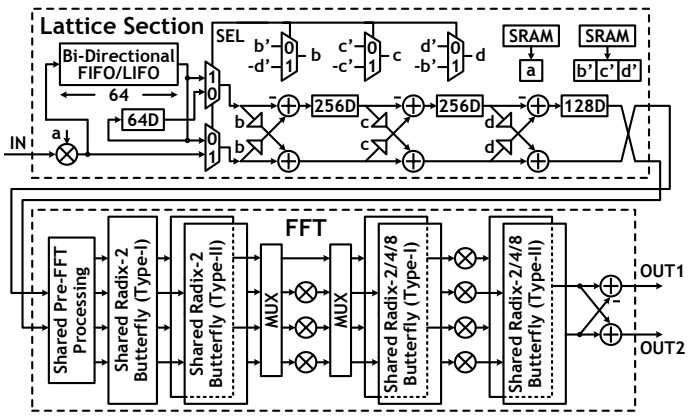


Figure 32.6.4: Circuit diagram of the EMAB block.

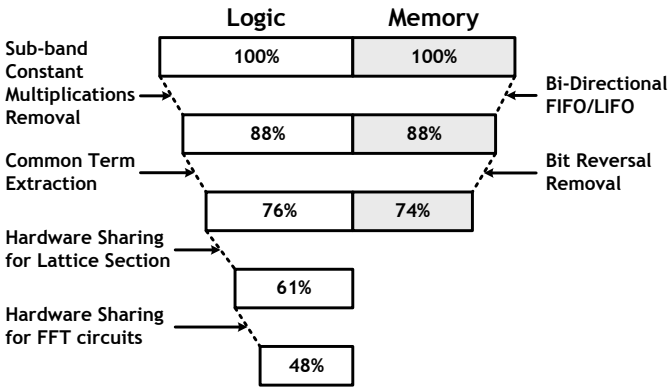
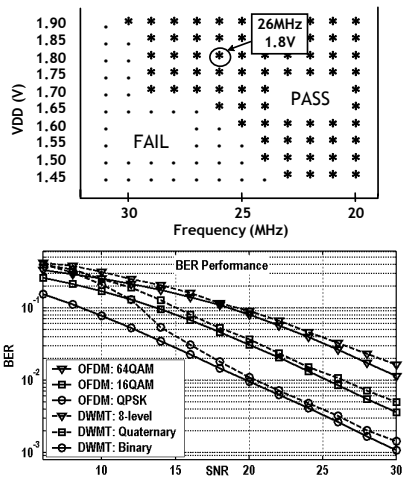


Figure 32.6.5: Summary of hardware reduction techniques in the EMAB block.



Chip Summary		
Technology		0.18 CMOS 1P6M
Area (mm^2)	Chip	3.42 × 3.42
	Core	2.50 × 2.50
Logic Gates		267K
SRAMs		60Kb
Supply Voltage		1.8 V
Nominal Clock Rate		25.6 MHz
Core Power Consumption		165 mW
Uncoded Bit Rate		51.2 / 102.4 / 153.6 Mb/s

Figure 32.6.6: Measurement results and chip summary.

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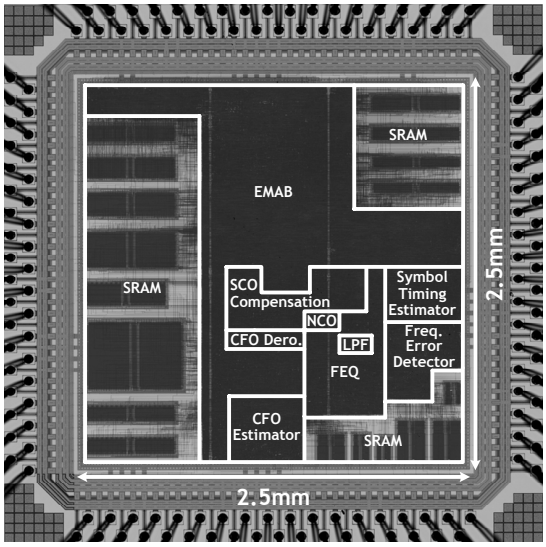

Figure 32.6.7: Chip micrograph.

